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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
STEVENS, ROBERT	
ART UNIT	**PAPER NUMBER**
2176	

DATE MAILED: 05/31/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/992,637	KIZHEPAT, GOVIND	
	Examiner	Art Unit	
	Robert Stevens	2176	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 March 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This action is responsive to communications: amendment filed 3/13/2006.

2. This action is **FINAL**.

3. The Office withdraws the previous rejections of the claims under 35 U.S.C. § 103(a), in light of the amendment.

4. The Office sets forth new rejections of the claims under 35 U.S.C. §§ 112-1st paragraph and 103(a), in light of the amendment.

5. Claims 1-33 are pending. Claims 1, 12, 23 and 29 are independent.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

7. **Claims 1-33 are rejected under 35 U.S.C. 112, first paragraph**, as failing to comply with the written description requirement. The claims contain subject matter

which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Independent claims 1, 12, 23 and 29 were amended to recite "function cycle". This terminology does not appear in the as-filed specification, and as such constitutes new matter. For the purposes of further examination, the terminology will be interpreted as a "clock cycle", which is inherent to computer-based processing.

Claims 2-11, 13-22, 24-28 and 30-33 are dependent upon claims 1, 12, 23 and 29, respectively, and therefore are likewise rejected.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. **Claims 1-33 are rejected under 35 U.S.C. 103(a)** as being unpatentable over Lynch (US Patent No. 5,930,492, filed Mar. 19, 1997 and issued Jul. 27, 1999, hereafter referred to as "Lynch") in view of Nosenchuck et al (US Patent No. 4,811,214, filed Dec. 22, 1998 and issued Oct. 29, 2002, hereafter referred to as "Nosenchuck").

Independent claim 1 states:

> *A data processing system, comprising:*
> *a plurality of functional units having respective inputs and outputs, and adapted to perform respective tasks using input data at the respective inputs and to supply output data at the respective outputs, within a function cycle;*
> *a plurality of routing units, responsive to respective routing control signals, by which data is steered among inputs and outputs of the plurality of functional units, routing units in the plurality of routing units being coupled to respective subsets of functional units in the plurality of functional units, wherein at least one of said respective subsets is different than another of said respective subsets; and*
> *control word distribution circuitry which supplies the routing control signals in parallel to the plurality of routing units to establish a route for a function cycle, where the route includes applying data output in the function cycle by a first functional unit in the plurality of functional units as input in the function cycle to a second functional unit in the plurality of functional units and applying data output by the second functional unit in the function cycle as input in the function cycle to a third functional unit in the function cycle.*

Lynch teaches the use of a plurality of pipeline stages in Figure 3, showing stages 1 through 4. Each stage represents plurality functional units, with inputs and outputs as shown in the figure. Figure 13 further shows data control and steering (i.e., routing) circuitry in Figure 13 #160. Lynch further discusses processing incorporating a pipeline of multiple stages (implementing function unit or group processing) in col. 3 lines 8-32, discussing pipelining data and control from first through third stages, it being

implied that processing actions occur on a clock cycle (i.e., function cycle) basis. See also col. 10 lines 65-67 discussing clock cycle execution.

However, Lynch does not explicitly disclose a plurality of routing units. Nosenchuck, though, discloses a hyperspace router in Figure 8 #80. Internal to the router is shown a plurality of routing units. Coupled to the hyperspace router is the MASNET #26, which connects to functional units as discussed in the Abstract.

It would have been obvious to one of ordinary skill in the art at the time of the invention to apply the teachings of Nosenchuck for the benefit of Lynch, because to do so would have enabled a system designer to implement powerful algorithms directly, as taught by Nosenchuck in the Abstract. These references were all applicable to the same field of endeavor, i.e., processing pipeline control and configuration.

Regarding dependent claims 2-4, Lynch discloses the use of multiplexers in Figure 2 #42 B and C, showing the well-known symbols for multiplexer elements. Lynch discloses the use of storage elements in Figure 1 #30 and 32, showing a register file and a buffer, respectively.

However, Lynch does not explicitly disclose a crossbar switch. Nosenchuck, though, discloses the use of a switching element in Figure 5A #70, showing a FLONET switch, it being merely an obvious variant as to the particular switching fabric employed.

It would have been obvious to one of ordinary skill in the art at the time of the invention to apply the teachings of Nosenchuck for the benefit of Lynch, because to do

so would have enabled a system designer to implement powerful algorithms directly, as taught by Nosenchuck in the Abstract. These references were all applicable to the same field of endeavor, i.e., processing pipeline control and configuration.

Regarding dependent claims 5-8, Lynch discloses control word logic for performing functions in col. 21 lines 15-25. Figure 13 further shows stages, comprised of processing functionality and controlled by control words and steering words, as shown in the interfacing of elements 160 and 164A-D, it being an obvious variant as to the specific control signals sent to the plurality of stages. Lynch does not disclose a plurality of explicit functional units. Nosenchuck, though, discloses a plurality of explicit functional units in Figure 4, showing an interconnection of functional units 1-5 (each referenced as #62).

It would have been obvious to one of ordinary skill in the art at the time of the invention to apply the teachings of Nosenchuck for the benefit of Lynch, because to do so would have enabled a system designer to implement powerful algorithms directly, as taught by Nosenchuck in the Abstract. These references were all applicable to the same field of endeavor, i.e., processing pipeline control and configuration.

Regarding dependent claims 9-11, Lynch discloses a pipelining of functional processing stages coupled to control and steering signal distribution circuitry in Figure 13, showing pipelined processing stages 164A-D and control/steering word circuitry #160.

Independent claim 12 states:

A data processing system, comprising:

a plurality of processing blocks having respective inputs and outputs, and adapted to perform respective processes using input data at the respective inputs and to supply output data at the respective outputs, within a function cycle;

a plurality of processing blocks, responsive to respective routing control signals for the plurality of processing blocks, by which data is steered among the inputs and outputs of the plurality of processing blocks, routing units in the plurality of routing units being coupled to respective subsets of processing blocks in the plurality of processing blocks, wherein at least one of said respective subsets of processing blocks is different than another of said respective subsets processing blocks; and

block level control word distribution circuitry which supplies control words for respective function cycles to the plurality of routing units, said control words including the routing control signals for the plurality of routing units;

wherein processing blocks in said plurality of processing blocks respectively include

a plurality of functional units having respective inputs and outputs, and adapted to perform respective processes using input data at the respective inputs and to supply output data at the respective outputs, within a block function cycle;

a plurality of unit level routing units, coupled to the plurality of functional units and responsive to respective routing control signals for the plurality of unit level routing units, by which data is steered among the inputs and outputs of the plurality of functional units, unit level routing units in the plurality of unit level routing units being coupled to respective subsets of functional units in the plurality of functional unit, wherein at least one of said respective subsets of functional units is different than another of said respective subsets of functional units; and

functional unit level control word distribution circuitry which supplies control words for respective block function cycles to the plurality of unit

level routing units, said control words including the routing control signals to establish a route in the block function cycle for the plurality of unit level routing units, where the route includes applying data output in the block function cycle by a first functional unit in the plurality of functional units as input in the block function cycle to a second functional unit in the plurality of functional units and applying data output by the second functional unit in the block function cycle as input in the block function cycle to a third functional unit in the block function cycle.

Lynch teaches the use of a plurality of pipeline stages in Figure 3, showing stages 1 through 4. Each stage represents plurality of processing units, with inputs and outputs as shown in the figure. Figure 13 further shows data control and steering (i.e., routing) circuitry in Figure 13 #160. It was implied that processing occurs on a clock cycle basis. Lynch further discusses processing incorporating a pipeline of multiple stages (implementing function unit or group processing) in col. 3 lines 8-32, discussing pipelining data and control from first through third stages, it being implied that processing actions occur on a clock cycle (i.e., function cycle) basis. See also col. 10 lines 65-67 discussing clock cycle execution.

However, Lynch does not explicitly disclose a plurality of different processing blocks. Nosenchuck, though, discloses a hyperspace router in Figure 8 #80. Internal to the router is shown a plurality of routing units. Coupled to the hyperspace router is the MASNET #26, which connects to functional units as discussed in the Abstract.

It would have been obvious to one of ordinary skill in the art at the time of the invention to apply the teachings of Nosenchuck for the benefit of Lynch, because to do so would have enabled a system designer to implement powerful algorithms directly, as

taught by Nosenchuck in the Abstract. These references were all applicable to the same field of endeavor, i.e., processing pipeline control and configuration.

Claims 13-21 are substantially similar to claims 2-10, respectively, and therefore likewise rejected.

Regarding claim 22, Lynch discloses the use of a clocking mechanism in col. 2 lines 40-47, discussing an advantage which enabled a clock speed increase - it being implied that clock-based processing is inherently synchronous.

Independent claim 23 states:

A method of processing data, in a data processing engine that includes a plurality of functional units, comprising:

providing a set of software routing control signals in parallel to a set of routing units in the data processing engine to specify a route for a function cycle among the plurality of functional units; and

routing data among the plurality of functional units according to the set of software routing control signals and performing tasks in the plurality of functional units using the route to produce a result, wherein routing units in the set of routing units are coupled to respective subsets of functional units in the plurality of functional units, wherein at least one of said respective subsets of functional units is different than another of said respective subsets of functional units, where the route includes applying data output in the function cycle by a first functional unit in the plurality of functional units as input in the function cycle to a second functional unit in the plurality of functional units, and applying data output by the second functional unit in the function cycle as input in the function cycle to a third functional unit in the block function cycle.

Lynch teaches the use of a plurality of pipeline stages in Figure 3, showing stages 1 through 4. Each stage represents plurality functional units, with inputs and outputs as shown in the figure. Figure 13 further shows data control and steering (i.e., routing) circuitry in Figure 13 #160. Lynch further discusses processing incorporating a pipeline of multiple stages (implementing function unit or group processing) in col. 3 lines 8-32, discussing pipelining data and control from first through third stages, it being implied that processing actions occur on a clock cycle (i.e., function cycle) basis. See also col. 10 lines 65-67 discussing clock cycle execution. Lynch describes an exemplary pipelining of processing in which outputs from one processing stage are provided as inputs to another processing stage in col. 3 lines 5-32, discussing processing and data flow among three stages of a processing pipeline.

However, Lynch does not explicitly disclose a plurality of routing units. Nosenchuck, though, discloses a hyperspace router in Figure 8 #80. Internal to the router is shown a plurality of routing units. Coupled to the hyperspace router is the MASNET #26, which connects to functional units as discussed in the Abstract.
It would have been obvious to one of ordinary skill in the art at the time of the invention to apply the teachings of Nosenchuck for the benefit of Lynch, because to do so would have enabled a system designer to implement powerful algorithms directly, as taught by Nosenchuck in the Abstract. These references were all applicable to the same field of endeavor, i.e., processing pipeline control and configuration.

Regarding claim 24, Lynch discloses the use of an x86-based architecture in col 14 line 31 and Table 1 of col. 29, it being well-known that x86 microprocessors were programmable in high level languages, which were an obvious variant of using microcode as in Table 1.

Claims 25-26 are substantially similar to claims 9-10, respectively, and therefore likewise rejected.

Regarding claims 27-28, Lynch teaches the use of a plurality of pipeline stages in Figure 3, showing stages 1 through 4, with each stage representing a plurality of functional units. Lynch further teaches the use of a steering word to specify connecting paths for pipeline stages in col. 5 lines 22-34. Lynch further discloses the use of a clocking mechanism in col. 2 lines 40-47, discussing an advantage which enabled a clock speed increase - it being implied that clock-based processing is inherently synchronous. Lynch, however, does not explicitly disclose a plurality of switches. Nosenchuck, though, discloses a switching network in Figure 5A, showing element #70, a FLONET switching network, it being implicit that a switching network is comprised of a plurality of switches.

It would have been obvious to one of ordinary skill in the art at the time of the invention to apply the teachings of Nosenchuck for the benefit of Lynch, because to do

so would have enabled a system designer to implement powerful algorithms directly, as taught by Nosenchuck in the Abstract. These references were all applicable to the same field of endeavor, i.e., processing pipeline control and configuration.

Independent claim 29 states:

> *A method of processing data in a data processing engine that includes a plurality of functional units, comprising:*
> *providing a first set of software routing control signals in parallel to a set of routing units in the data processing engine to specify a first data path according to a first configuration of the plurality of functional units for a first function cycle, wherein routing units in the set of routing units are coupled to respective subsets of functional units in the plurality of functional units, wherein at least one of said respective subsets of functional units is different than another of said respective subsets of functional units, where the first data path includes applying data output in the first function cycle by a first functional unit in the plurality of functional units as input in the first function cycle to a second functional unit in the plurality of functional units, and applying data output by the second functional unit in the first function cycle as input in the first function cycle to a third functional unit in the block function cycle;*
> *performing tasks in said plurality of functional units using the first data path in the first function cycle;*
> *providing a second set of software routing control signals in parallel to said set of routing units to specify a second data path according to a second configuration of the plurality of functional units for a second function cycle, whereby the plurality of functional units is reconfigured to perform a different function; and*
> *performing tasks in said plurality of functional units using the second data path to accomplish said different function in the second function cycle.*

Lynch teaches the use of a plurality of pipeline stages in Figure 3, showing stages 1 through 4. Each stage represents plurality functional units, with inputs and outputs as shown in the figure. Figure 13 further shows data control and steering (i.e., routing) circuitry in Figure 13 #160. Lynch further discusses processing incorporating a

pipeline of multiple stages (implementing function unit or group processing) in col. 3 lines 8-32, discussing pipelining data and control from first through third stages, it being implied that processing actions occur on a clock cycle basis. See also col. 10 lines 65-67 discussing clock cycle execution. Lynch describes an exemplary pipelining of processing in which outputs from one processing stage are provided as inputs to another processing stage in col. 3 lines 5-32, discussing processing and data flow among three stages of a processing pipeline.

However, Lynch does not explicitly disclose a plurality of routing units. Nosenchuck, though, discloses a hyperspace router in Figure 8 #80. Internal to the router is shown a plurality of routing units. Coupled to the hyperspace router is the MASNET #26, which connects to functional units as discussed in the Abstract.
It would have been obvious to one of ordinary skill in the art at the time of the invention to apply the teachings of Nosenchuck for the benefit of Lynch, because to do so would have enabled a system designer to implement powerful algorithms directly, as taught by Nosenchuck in the Abstract. These references were all applicable to the same field of endeavor, i.e., processing pipeline control and configuration.

Claims 30-31 are substantially similar to claims 9-10, respectively, and therefore likewise rejected.

Claim 32 is substantially similar to claim 27, and therefore likewise rejected.

Claim 33 is substantially similar to claim 24 and therefore likewise rejected.

Response to Arguments

10. Applicant's arguments have been fully considered but they are considered moot in light of the use of new art in the rejections of the claims. It is noted that the amendment substantially changes the scope of the claimed subject matter.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US Patents

McMillen et al	6,473,827
Muller et al	6,256,740
Chow et al	6,594,698
Kim	6,304,568
Frazier	6,078,990
Bartkowiak et al	5,771,362
Swaney	5,245,705
Pflum	5,790,821
Gifford	4,891,787

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Robert Stevens whose telephone number is (571) 272-4102. The examiner can normally be reached on M-F 6:00 - 2:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Heather R. Herndon can be reached on (571) 272-4136. The current fax phone number for the organization where this application or proceeding is assigned is 703-872-9306. Additionally, the main number for Technology Center 2100 is (571) 272-2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Robert Stevens
Art Unit 2176
Date: May 24, 2006

rs

William L. Bashore
WILLIAM BASHORE
PRIMARY EXAMINER
5/29/2006